REMARKS

Claims 1-15 remain in the application. Claims 1-4, 6-9 and 11-14 stand rejected. Claims 5, 10 and 15 have been objected to as dependent upon rejected claims but are otherwise allowable. Applicants appreciate the indication of allowable subject matter.

The Examiner has rejected claims 1-4, 6-9 and 11-14 under 35 U.S.C. 102 as anticipated by Gersbach et al. Applicants respectfully request reconsideration of this rejection.

Each of the independent claims, in the last two or three lines, requires changing "said output clock signal in accordance with a relationship between said received data signal and said output clock signal."

This limitation is reflected in Figure 2 of the drawings of this application in which the output clock CLK0 on line 42 is fed back and compared in phase detect/compare block 50 with the incoming received signal RX SIGNAL. In each of the independent claims the change in output clock signal is triggered by the relationship between the "received to data signal and said output clock signal."

Gersbach et al do not operate in a way that meets these claim limitations. Specifically, in Gersbach et al, the output of the multiplexer 30, identified as EXTRACTED CLOCK is not fed back and compared with the receive clock and signal data. Rather, a very complex set of circuitry comprising sorting circuits 20, barrel shifter 26, counters 22, control logic 24 and up/down counter 28 are employed to generate a control signal to multiplexer 30 which selects which of the phases from the delay element 18 are selected to be the applied to the EXTRACTED CLOCK

output. In paragraph [0003] of the specification, one of the problems overcome by the present invention is the expense associated with clock recovery circuits. The Gersbach et al circuit is not only complex but it would be very expensive to implement. In contrast, the claimed invention shown in Figure 2 of this application has a very simple architecture which is the result of comparing the output CLK0 with the incoming signal in phase detect/compare 50.

Therefore, the claim limitations which expressly require that the output clock signal be adjusted in accordance with the relationship between "said received data signal and said output clock signal" has great value which results in both lessening of expense and in simplicity of construction. Therefore, Gersbach et al do not anticipate any of the independent claims and a fortiori none of the dependent claims. Further, modifying Gersbach et al would not be obvious because there is no apparent way to eliminate all of the complex circuitries that results from using sorting circuits 20, barrel shifter 26, counters 22, control logic 24 and up/down counter 28.

For the reasons indicated, the Examiner has not set forth a prima-facie case of anticipation and has provided no reason for modifying Gersbach et al to operate as the claimed invention requires. For these reasons, applicants respectfully request that the Examiner reconsider his rejection and withdraw it.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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In re Patent Application of:
KLIESNER ET AL
Serial No. **10/620,151**
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Respectfully submitted,

/david l. stewart/
Reg. No. 37,578

Customer No.: 27975

Telephone: (407) 841-2330

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